Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A process for cleaning an integrated circuit package surface, comprising:

introducing said integrated circuit package inside a plasma chamber; and

exposing said integrated circuit package to a ~~noble-gas-ion~~physical plasma for a selected time and strength to remove an upper layer of material from the package.

2. (Original) The cleaning process according to Claim 1, wherein said physical plasma has a halogen-type behavior.

3. (Currently Amended) The cleaning process according to Claim 1 wherein said ~~noble-gas-ion~~ physical plasma is obtained in the presence of a pure noble gas.

4. (Original) The cleaning process according to Claim 3, wherein said noble gas is argon.

5. (Currently Amended) The cleaning process according to Claim 1 wherein said step of exposing said integrated circuit to a ~~noble-gas-ion~~physical plasma comprises the step of energizing said plasma by applying the following energization parameters: energization time, between 12 and 15 seconds; energization power, between 140 and 160 W; and plasma chamber pressure, between 190 and 210 millitorr.

6. (Original) The cleaning process according to Claim 1, further including:

applying a continuous voltage to obtain ionization of said plasma.

7. (Original) The cleaning process according to Claim 1, further including:

applying a radio-frequency voltage at a frequency of between 1 kHz and 100 GHz, to obtain ionization of said plasma.

8. (Currently Amended) The cleaning process according to Claim 1 wherein the exposing of said integrated circuit package to a physical plasma occurs in a single exposure.

9. (Original) The process according to Claim 1 wherein the package is composed of a ceramic material.

10. (Previously Presented) The manufacturing process according to Claim 1, further comprising placing a pattern of ink marking on said package for marking said package using a laser ink marking technique.

11. (Original) The process according to Claim 1 wherein the package is composed of a plastic material.

12. (Original) The process according to Claim 1 wherein the package is composed of an epoxy resin material.

13. (Original) The process according to Claim 1 wherein the package includes exposed metal components.

14. (Previously Presented) A process for manufacturing an integrated circuit, comprising:

cleaning of an integrated circuit package surface by introducing the packaged integrated circuit into a plasma chamber;

exposing the package surface to a noble gas ion plasma;

removing a layer of material from the package surface to clean the upper surface of the package; and

ink marking said package surface.

15. (Original) The manufacturing process according to Claim 14, wherein said ink marking process is carried out using a laser ink marking technique.

16. (Original) The process according to Claim 14 wherein the package is composed of a ceramic material.

17. (Original) The process according to Claims 14 wherein the package is composed of a plastic material.

18. (Original) The process according to Claim 14 wherein the package is composed of an epoxy resin material.

19. (Original) The process according to Claim 14 wherein the package includes exposed metal components.

20. (Previously Presented) The cleaning process according to Claim 1, wherein said noble gas is helium.

21. (New) The process of claim 1 wherein the physical plasma is a noble gas ion plasma.

22. (New) A process, comprising:

introducing an integrated circuit package into a plasma chamber; and

cleaning the package, the cleaning step including exposing the package to only one plasma etch step.

23. (New) The process of claim 22 wherein the one plasma etch step is a physical etch step.

24. (New) The process of claim 22, further comprising marking the integrated package.

25. (New) The process of claim 22 wherein the integrated circuit package is one of a frame of integrated circuit packages cleaned during the cleaning step.

26. (New) The process of claim 25 wherein the frame of integrated circuit packages is one of a plurality of frames of integrated circuit packages, the process further comprising repeating the cleaning step a plurality of times, each repetition directed to cleaning a different one of the plurality of frames of integrated circuit packages.

27. (New) The process of claim 25 wherein the integrated circuit package is one of a batch of integrated circuit packages cleaned during the cleaning step.

28. (New) The process of claim 22 wherein the one plasma etch step includes an energization time of 12-15 seconds.

29. (New) The process of claim 22 wherein the one plasma etch step is performed using a noble gas ion plasma.

30. (New) The process of claim 22 wherein the noble gas consists of a single noble gas.